REMARKS

In response to the Office Action mailed February 7, 2005, claims 5 and 8 have been amended to overcome their rejection under 35 U.S.C. §112. Claims 3 and 4 were rejected under 35 U.S.C. §102 but these claims have also been amended to overcome the Examiner's rejection.

Separate and apart from the patentability of the pending claims, the applicant wishes this record to reflect its belief that the subject matter *claimed* in Taguchi (U.S. Pat. No. 6,480,030) is believed to be different than anything that is currently made, used or sold in the U.S. by the applicant.

Paraphrased, claim 3 now recites that the claimed control means compares an external reference voltage to an internal reference voltage and outputs a control signal to select one of the first and second input buffers. Support for the amendment to claim 3 can be found in at least paragraph [0040].

The Applicant submits that claim 3 as amended avoids the Taguchi reference (U.S. Pat. No. 6,480,030). Paraphrased, claim 3 recites the selection of a buffer based on the comparison of an external reference voltage to an internal reference voltage. As for claim 4, it recites that the buffers of claim 3 are a CMOS buffer and a differential buffer, that one of them is selected based on the results of a comparison of the two different reference voltages recited in claim 3, i.e., the comparison of an external reference voltage to an internal reference voltage.

The Applicant submits that Taguchi does not show the selection of one of two different buffers based on the results of a comparison of two different reference voltages. Rather, Taguchi teaches the selection of a buffer based on the selection of a signal to a single reference voltage.

Paraphrased, claim 5 now recites that the control section enables operation of the CMOS buffer when an input signal that is *at least one* of a command signal and an address signal, is not being input from an external source. Support for the amendment to claim 5 is found in at least paragraphs [0008] – [0010] and [0037] and [0052].

Claim 8 has been amended to delete ambiguous language that recited when the CMOS buffer operates. The terms of claim 8 were both confusing and unnecessary.

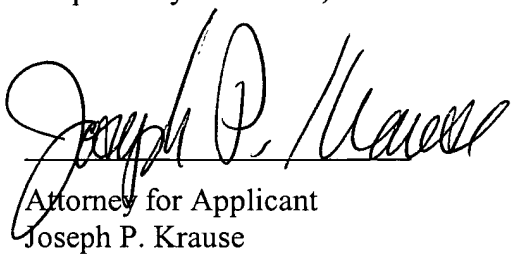
That the CMOS buffer operates when the control signal is not between the first and second reference potentials is inherent and made clear in the specification. The claim was also amended to delete the word "located" because it was syntactically incorrect. Signal levels, *per se*, are not "located."

Claims 1-2 were allowed. Claims 6-10 were stated as being allowable if they are re-written to overcome the rejections of claims 5 and 8 under §112. The Examiner did not specifically identify claim 5 as being allowable if it were to be rewritten, but since the only reason that was given for it's rejection was it's rejection under 35 U.S.C. §112, and since that rejection has been overcome, it is respectfully submitted that claim 5 is also in condition for allowance.

Claim 1 has been superficially amended to correct typographical errors. In particular, claim 1 has been amended to change the semi-colon after the "comprising" transition to a colon. It was also amended to change the word "ENABLE" to lower case. It is otherwise identical to its condition at filing.

Since claims 1 and 2 are allowable, and since claims 5 and 8 have been amended to overcome their rejection under §112, the applicant submits that claims 1-2 and 5-10 are in condition for allowance.

Respectfully submitted,



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